RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2815

PATENT APPLICATION
Docket No.: 9903-075
Client Ref. No.: S03US009

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Dong-Han KIM		
Serial No.:	10/801,501	Examiner:	Diaz, Jose R.
Filed:	March 12, 2004	Group Art Unit:	2815
Confirmation No.:	1864		
For:	SEMICONDUCTOR CHIP WITH TEST PADS AND TAPE CARRIER PACKAGE USING THE SAME		

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20060319, dated March 23, 2006, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

IN THE CLAIMS

1. (Currently amended) A semiconductor chip comprising:

a plurality of outer edges;

a peripheral area located adjacent to the outer edges; and

a main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits,

wherein the peripheral area includes chip pads connected to the integrated circuits, ~~and also~~ a plurality of test pads electrically being connected to the integrated circuits for testing electrical properties of the integrated circuits, the respective chip pads, the respective test pads, ~~and~~ the respective chip pads and test pads being arranged in four rows at substantially uniform intervals, the chip pads being arranged in each of the rows adjacent the main circuit area of the semiconductor chip, and the test pads being located within each of the rows of chip pads, and the test pads are substantially the same dimensional size as the chip pads.

2. (Cancelled)

3. (Cancelled)

4. (Currently amended) The semiconductor chip of claim ~~2~~ 1, wherein the test pads are located at the ends of each of the rows of chip pads.

5. (Currently amended) The semiconductor chip of claim ~~2~~ 1, wherein the configuration of the main circuit area is arranged to form corners, and the test pads are located near the corners of the main circuit area.

6. (Currently amended) The semiconductor chip of claim 1, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within each of the rows of chip pads.

7. (Currently amended) The semiconductor chip of claim ~~2~~ 1, wherein the test pads are arranged between chip pads within each of the rows of chip pads.

8. (Cancelled)

9. (Cancelled)

10. (Original) The semiconductor chip of claim 1, which comprises one of an edge-pad-type chip and a center-pad-type chip.

11. (Currently amended) A tape carrier package comprising:

a semiconductor chip comprising a plurality of outer edges, a peripheral area located adjacent to the outer edges, and an main circuit area located within the confines of the peripheral area, the main circuit area including integrated circuits, the peripheral area including chip pads connected to the integrated circuits, and a plurality of test pads electrically connected to the integrated circuits for testing the electrical properties of the integrated circuits, the respective chip pads, the respective test pads, and the respective chip pads and test pads being arranged in four rows at substantially uniform intervals, the chip pads being arranged in each of the rows adjacent the main circuit area of the semiconductor chip, and the test pads being located within each of the rows of chip pads, and the test pads are substantially the same dimensional size as the chip pads; and

a tape wiring substrate.

12. (Cancelled)

13. (Cancelled)

14. (Currently amended) The tape carrier package of claim ~~12~~ 11, wherein the test pads are located at the ends of each of the rows of chip pads.

15. (Currently amended) The tape carrier package of claim ~~12~~ 11, wherein the configuration of the main circuit area is arranged to form corners, and the test pads are located near the corners of the main circuit area.

16. (Currently amended) The tape carrier package of claim 11, wherein the chip pads are arranged in rows parallel to at least one set of opposed outer edges of the semiconductor chip, and the test pads are arranged within each of the rows of chip pads.

17. (Currently amended) The tape carrier package of claim ~~12~~ 11, wherein the test pads are arranged between chip pads within each of the rows of chip pads.

18. (Cancelled)

19. (Original) The tape carrier package of claim 11, wherein the tape wiring substrate comprises an insulating base film, wiring patterns formed on the insulating base film, leads formed integrally with the wiring patterns, and dummy leads electrically isolated from the wiring patterns.

20. (Original) The tape carrier package of claim 19, which further comprises bumps connecting the chip pads to the corresponding leads and the test pads to the dummy leads.

REMARKS

Claims 1-20 are pending.

Claims 1-20 are rejected.

Claims 2, 3, 8, 9, 12, 13, and 18 have been cancelled.

Claims 1, 4-7, 10, 11, 14-17, 19 and 20 are presented for reconsideration.

Claim Rejections – 35 U.S.C. § 102

Claims 1-6 and 9-10 remain rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda U.S. Patent No. 6,127,729 ("Fukuda').

Applicant traverses this rejection. Fukuda does not teach or suggest the claimed invention for the reasons set forth in detail below.

The amended claims recite that the test pads are arranged between chip pads within each of the rows of chip pads. In Fukada, the test pads are not arranged between chip pads within each of the rows of chip pads. The amended claims recite that the test pads are substantially the same dimensional size as the chip pads. In Fukada, the test pads are not substantially the same dimensional size as the chip pads. In amended claims 4 and 14, the test pads, which are the same dimensional size as the chip pads, are located at the ends of each of the rows of chip pads. In Fukada, test pads which are not the same dimensional size as the chip pads are located at the ends of each of the rows of chip pads.

In order for a prior art reference to anticipate a claim under 35 USC 102 (e), each and every element of the claimed invention must be identically shown in the reference. For the reasons set forth above, the Examiner has not made a prima facie case of anticipation.

Claims 1-20 remain rejected under 35 U.S.C. 102(b) as being anticipated by Aiki et al JP 2002-303653 ("Aiki").

Applicant traverses this rejection. Aiki does not teach or suggest the claimed invention for the reasons set forth in detail below.

The amended claims recite that the respective chip pads and test pads are arranged in four rows at substantially uniform intervals, and that the test pads are located within each of the four rows of chip pads. In Aiki, the respective chip pads and test pads are not arranged in four rows at substantially uniform intervals. Also in Aiki, the chip pads and the test pads are not located within each of the four rows of chip pads. In claims 7 and 17, for example, the test pads are arranged between chip pads within each of the four rows of chip pads. In Aiki, the test pads are not arranged between chip pads within each of the four rows of chip pads.

In order for a prior art reference to anticipate a claim under 35 USC 102 (e), each and every element of the claimed invention must be identically shown in the reference. For the reasons set forth above, the Examiner has not made a prima facie case of anticipation.

For the foregoing reasons, reconsideration and allowance of claims 1, 4-7, 10, 11, 14-17, 19 and 20 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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